I have the following points to be updated gradually.

1. Lab TUTORIALS & SCRIPTS
   1. The long Lab Script should be cleaned off and minimized, and may be split into multiple session tutorials to be distributed on a session requiring that tutorials. For example the long script may be divided into Lab Introduction, DLX Tutorial, ModelSim Tutorial, Xilinx Tutorial, XPower Tutorial, ASIPmeister Tutorial etc. Each session may consist of a separate tutorial and an exercise sheet. This will be much easier and less time consuming for the students.
      1. Separate Session Tutorial
      2. Separate Session Exercises (with fill in the blanks or tables in excel or libracalc for each exercise)
      3. Grade/attendance Sheet
   2. Or we can clean big Script.
      1. Lab Tutorial
      2. Separate Session Exercises (with fill in the blanks or tables in excel or libracalc for each exercise)
      3. Grade/attendance Sheet
   3. We can add flowchart of lab, lab policies section.
   4. Flow chart may consists of:
      1. Start-up
      2. Introduction to Assembly
      3. Introduction to ModelSim
      4. Custom Instruction Profiling & Defining new Instructions (
         1. Simulating an Application
         2. Optimizing the application
         3. Realizing the application in Hardware
      5. Performance, Power and Area Estimation
      6. CoSy Compiler (Executing new Instructions in C program)
      7. Optimize & benchmark an Application using all the steps above
2. TOOLS USED
   1. ASIPmeister to be upgraded
   2. CoSy Compiler to be upgraded
3. Web page of LAB to be updated with some kind of flow chart and recent pictures.
4. Currently Sessions are divided as:
   1. Session 0 Laboratory Introduction
   2. Session 1 Simulation of DLX-Assembly Programs
   3. Session 2 ASIP Meister and ModelSim
   4. Session 3 Bubble Sort – Simulation
   5. Session 4 Bubble Sort – Optimisation
   6. Session 5 Hardware Implementation
   7. Session 6 Power Estimation
   8. Session 7 CoSy Compiler
   9. Session 8 ADPCM: Adaptive Differential Pulse Code Modulation
5. Suggestions for & Bottlenecks for Individual Sessions
   1. bs\_bgeu\_opt is not working for Hardware
   2. 4.2. Explicitly, we should mention which execution time (ModelSim/UART) is used during bubbleSort\_LCD\_HW/SW.s.
   3. LCD is not showing anything.
   4. Small Description about the Tiny Board with reset and UART interface. Crystal/Frequency Used?
   5. Finding critical path and peak power
   6. CoSy compiler is not working for modified CPUs
   7. Remove some un-necessary sentences from tutorials and script
   8. Executions times or cycles are not clear where to get from? ModelSim or FPGA Board
   9. More accurate critical path explanations
   10. Scripts to automate ModelSim and stuff like that?
   11. # of cycles for last sessions is not working in FPGA?
   12. Scripts for XPower, Xilinx ise, and ModelSim to speed up the process.
   13. Add X2Go introduction sections into script
6. Some Questions
   1. Which files are required for whole flow?
   2. Which assembly file is used during execution? projectname.asm file
   3. Flow of Makefile?
   4. DOC files
   5. CoSy Compiler? If we are not able to makeCoSy for modified CPUs, then what is the actual role of CoSy Compiler session? Why not, just take CoSy Compiler executable for dlx\_basis.pdb and remove processing some files on i80pc06 (CoSy Computer).

We can add synthesis, place & route and power estimation using Design Compiler, Cadence Encounter, & PrimeTime respectively. And use Xilinx ISE (FPGA) only for hardware realization of the applications. We can combine Session 3&4 into one. And Session 4&5 into one and add Design Compiler, Encounter PrimeTime Stuff.

Step by Step Procedure for

1. Setting up project directory and environmental settings
2. Using ssh or x2go client
3. Using ASIPmeister
4. Using dlxsim, Modifying dlxsim
5. Using ModelSim (with GUI n scripts)
6. Using Xilinx ISE (with GUI n scripts)
7. Using XPower (with GUI n scripts)

Tutorials